WHAT IS CLAIMED IS:

1. An integrated chip package, comprising:

Sub A1

at least one semiconductor chip having a first surface and a second surface;

an intermediate substrate electrically coupled via conductive bumps to the first surface of the at least one semiconductor chip

a package substrate having a first surface electrically coupled to the intermediate substrate via a plurality of bonding wires; and

a heat sink thermally coupled to the second surface of the semiconductor chip.

2. The integrated chip package of Claim 1 wherein the second surface of the at least one semiconductor chip is adhesively bonded to the heat sink.

3. The integrated chip package of Claim 1 wherein the heat sink is substantially thermally isolated from the package substrate.

4. The integrated chip package of Claim 1 wherein the intermediate substrate is formed from a material selected from the group consisting of silicon, polysilicon, and glass.

5. The integrated chip package of Claim 1 wherein the intermediate substrate includes at least one capacitor electrically coupled to the at least one semiconductor chip.

6. The integrated chip package of Claim 5 wherein the at least one capacitor is a trench capacitor having a dielectric selected from the group consisting of nitride oxide and oxide.

7. The integrated chip package of Claim 1 wherein the conductive bumps are formed from a material selected from the group consisting of Pb/Sn solder, Au, Ag, alloys of Au and Ag, and metallic coated polymeric studs.

8. The integrated chip package of Claim 1 wherein the intermediate substrate includes a circuit plane selected from the group consisting of power planes, ground planes, and interconnect planes.

9. The integrated chip package of Claim 1 wherein at least two semiconductor chips are electrically coupled to one intermediate substrate; and

the intermediate substrate further includes at least one electrical plane for electrically interconnecting the at least two semiconductors.

10. The integrated chip package of Claim 9 wherein the at least one electrical plane is selected from the group consisting of power planes, ground planes, and interconnection planes.

11. The integrated chip package of Claim 1 wherein the package substrate includes conductive pads on a second surface to electrically connect the integrated chip package to a circuit board via conductive bumps.

12. The integrated chip package of Claim 1 further comprising a support material arranged between the package substrate and the intermediate substrate.

13. A method of forming an integrated chip package, comprising:

providing a semiconductor chip having a conductor pattern on a first surface;

electrically coupling the conductor pattern on the semiconductor chip to an intermediate substrate via a first set of conductive bumps;

thermally coupling a second side of the semiconductor chip to a heat sink; and

electrically coupling the intermediate substrate to a first surface of a package substrate via a plurality of bond wires.

14. The method of Claim 13 further including adhesively bonding the first surface of the semiconductor chip to the heat sink.

15. The method of Claim 13 further including thermally isolating the heat sink from the package substrate.

16. The method of Claim 13 further including forming the intermediate substrate from a material selected from the group consisting of silicon, polysilicon, and glass.

17. The method of Claim 13 further including attaching at least one capacitor to the intermediate substrate such that the at least one capacitor is electrically coupled to the at least one semiconductor chip.

18. The method of Claim 17 wherein the at least one capacitor is a trench capacitor.

19. The method of Claim 13 further including forming a circuit plane on the intermediate substrate, wherein the circuit plane is selected from the group consisting of power planes, ground planes, and interconnect planes.

20. The method of Claim 13 further including forming conductive pads on a second surface of the package substrate operable to electrically couple the integrated chip package to a circuit board via a second set of conductive bumps.

21. The method of Claim 13 further including electrically coupling at least two semiconductor chips to one intermediate substrate; and

forming an electrical plane on the intermediate substrate for electrically interconnecting the at least two semiconductors.

22. An integrated chip package, comprising:

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at least one semiconductor chip configured for flip chip mounting, having a first surface and a second surface;

a package substrate having a first surface and a second surface, the package substrate second surface to electrically couple the integrated chip package to a circuit board via conductive bumps;

a flip chip conversion means electrically coupled between the at least one semiconductor chip first surface and the package substrate first surface; and

a means for sinking heat from the second surface of the semiconductor chip.

23. The integrated chip package of Claim 22 further including means for adhesively bonding the first surface of the semiconductor chip to the heat sinking means.

24. The integrated chip package of Claim 22 further including means for thermally isolating the heat sinking means from the package substrate.

25. The integrated chip package of Claim 22 further including forming the flip chip conversion means from a material selected from the group consisting of silicon, polysilicon, and glass.

26. The integrated chip package of Claim 22 wherein the flip chip conversion means includes at least one means for filtering electrical power electrically coupled to the at least one semiconductor chip.

27. The integrated chip package of Claim 22 wherein the flip chip conversion means includes a means for electrically interconnecting.

28. The integrated chip package of Claim 22 wherein the second surface of the package substrate includes conductive pads for electrically interfacing to the conductive bumps.